REMARKS

Claims 32, 34-36, 38-40, 42-45 and 47-83 are pending. In the Office Action dated August 10, 2007 (the "Office Action"), the Examiner objected to claims 50-83 for informalities and rejected claims 36, 45, 57 and 67 under 35 U.S.C. § 112, second paragraph, for failing to distinctly claim the subject matter. The Examiner further rejected claims 32, 34, 35, 38-40, 42-44, 47-56, 58-66 and 68-83 under 35 U.S.C. § 102(a) as being anticipated by the publication entitled, *Intel MultiProcessor Specification* ("Intel") and also as being anticipated by U.S. Patent No. 5,884,091 to Ghori et al. ("Ghori").

Applicants respectfully remind the Examiner that consideration of a cited reference, previously filed May 24, 2004, is still requested. The reference cited, "Open VMS DCL Dictionary", was originally cited by Examiner Samuel Broda in the parent application and then cited by Applicants in this instant application on May 24, 2004. Per the Examiner's request in the Office Action dated August 7, 2006, Applicants supplied a copy of the reference with their response filed on November 13, 2006, along with a copy of the originally form PTO-892 from Examiner Broda. Applicants request Examiner's consideration and return of the same.

With respect to the objection of claims 50-83 for informalities, Applicants clarify the pending system claims are not limited to "purely software," and are not directed to "software per se." All the pending claims are directed to statutory subject matter.

With respect to the Examiner's rejection of claims 36, 45, 57, and 67 under 35 U.S.C. 112, second paragraph, claims 36 and 45 have been amended to overcome the rejection. Claims 57 and 67, however, appear to have sufficient antecedent basis from claims 56 and 66, respectively, and have not been amended. The Examiner's rejection of these claims under 35 U.S.C. 112, second paragraph, should be withdrawn.

As previously mentioned, claims 32, 34, 35, 38-40, 42-44, 47-56, 58-66 and 68-83 have been rejected by the Examiner under 35 U.S.C. § 102(a) as being anticipated by Intel.

Applicants maintain arguments from the previously submitted responses, and have the following additional arguments.

Claim 32 is patentably distinct from Intel because it fails to disclose the combination of limitations recited by claim 32. For example, Intel fails to disclose a method for selecting a compatible processor for addition to a multiprocessor computer that includes, among other things, executing a computer program comparing identifying information for each current processor in the multiprocessor computer with accessed processor compatibility information to determine the processors that are compatible with each current processor and providing

information identifying the processors that are compatible with each current processor before adding the new processor to the multiprocessor computer.

As described in the previously submitted responses, Intel is a specification intended to provide a multiprocessor computing interface standard that allows for the extension of the PC/AT platform to a multiprocessor realm while still maintaining binary compatibility with legacy single processor platforms. In particular, the specification describes data structures used to define the configuration of a multiprocessor system. These data structures are the "MP Configuration Table" and "Floating Point Structure." See Figure 4-1, pg. 4-1. The Floating Point Structure is a data structure containing a physical address pointer to the MP Configuration Table and is located in one of three possible locations in system memory. The MP Configuration Table is a configurable and optional data structure used to store information about the multiprocessor configuration including information about advanced programmable interrupt controllers, processors, buses and interrupts. The MP Configuration Table is filled in by the BIOS after it executes a CPU ID procedure on each of the processors in the system. See pg. 4-8. After the MP Configuration Table is configured and the operating system is loaded, the information in the table may be used by the OS. Intel suggests that the information may be used to "configure the operating system." See pg. B-2. The MP Configuration table as disclosed by Intel is intended to allow the operating system to "configure itself." See pg. B-7. The MP Configuration Table is filled with information about each of the processors present in the system at the time the BIOS executes the CPU ID. Compatibility with processors that are not present, for example, a processor that has yet to be added to the multiprocessor computer, is not provided.

The Examiner argues that "Intel teaches that the BIOS provides such information before the processor is added to the multiprocessor computer as a functioning new processor," citing to Table 4-5 of Intel. See the Office Action at page 22. Table 4-5, however, is a key to the CPU signature information obtained from each processor present in the system at the time the CPU ID procedure is executed by the BIOS. See Table 4-4. For example, if the 4-bits of information for the family is 0100 and the 4-bits of information for the model is 0101 sent by a processor in response to the CPU ID operation, the processor can be identified using Table 4-5, as an IntelSX2 Processor. The resulting information does not identify processors that are compatible but identifies the processors that are already in the system at the time the CPU ID operation is executed.

Claim 40 is similarly patentable over Intel. Claim 40 recites a method of selecting a compatible processor for addition to a multiprocessor computer that includes, among

other things, providing identifying information indicative of the identify of the new processor before adding the new processor to the multiprocessor computer, executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the accessed processor compatibility information to determine the processors that are compatible with each current processor, the computer program further comparing the identifying information for the new processor with the processors determined to be compatible with each current processor, and further providing an indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer. As previously discussed, Intel teaches filling the MP Configuration table with information for each of the processors existing in the computer system at the time a CPU ID operation is executed by the BIOS. None of the information entered in the MP Configuration table, however, provides information identifying the identify of a new processor before adding it to the computer system. Intel merely provides information for the processors already in the computer system.

Intel further fails to disclose the combination of limitations recited claim 50. For example, Intel fails to disclose a system for selecting a new processor for addition to a multiprocessor computer that includes, among other things, a fourth component that provides information identifying the processors that are compatible with each current processor before adding the new processor to the multiprocessor computer. Intel at most describes a computer system that can obtain information about each of the existing processors in the system and compile that information in an MP Configuration table. The Examiner has argued that Table 4-5 represents information of compatible processors before a new compatible processor is added to the computer system. See the Office Action at page 22. This, however, overstates the descriptive value of Table 4-5. As previously discussed, Table 4-5 provides information to decode the CPU signature information that processors already in the computer system provide in response to a CPU ID operation. The information in Table 4-5, however, does not provide information identifying the processors that are compatible with each current process before adding a new processor to the computer system.

Claim 60 is also patentably distinct from Intel. Claim 60 recites a system for selecting a new processor for addition to a multiprocessor computer containing at least one current processor that includes, among other things, a second component allowing identifying information to be provided that identifies the new processor before adding the new processor to the multiprocessor computer, a fourth component coupled to first, second and third components to compare the identifying information for the new processor with the compatibility information

to determine processors that are compatible with each current processor, and a fifth component that provides an indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer. Intel does not describe components for the computer system that allows identifying information to be provided that identifies the new processor before adding the new processor or that provides and indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer. Intel describes at most obtaining information for the processors currently in a system and populating an MP Configuration table with that information. Providing information for processors that would be compatible with the existing processors is not described, however.

Claims 70 and 76 are also patentably distinct from Intel because Intel fails to describe the combination of limitations recited by the respective claim. Claim 70 recites a computer-readable medium containing instructions for causing a computer system to use processor compatibility information to select a new processor for addition to a multiprocessor computer containing at least one current processor that includes, among other things, executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible with each current processor and providing information identifying the processors that are compatible with each current processor before adding the new processor to the multiprocessor computer. Claim 76 recites a computer-readable medium containing instructions for causing a computer system to use processor compatibility information to select a new processor for addition to a multiprocessor computer containing at least one current processor that includes providing identifying information indicative of the identity of the new processor before adding the new processor to the multiprocessor computer, executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible with each current processor, the computer program further comparing the identifying information for the new processor with the processors determined to be compatible with each current processor, and providing an indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer. The previous discussion of Intel with respect to claims 32, 40, 50, and 60 are relevant to the patentability of claims 70 and 76 as well.

For the foregoing reasons, claims 32, 40, 50, 60, 70, and 76 are patentable over Intel. The claims depending therefrom are similarly patentable based on their dependency from

a respective allowable base claim. Therefore, the Examiner's rejection of claims 32, 34, 35, 38-40, 42-44, 47-56, 58-66 and 68-83 under 35 U.S.C. 102(a) as being anticipated by Intel should be withdrawn.

As previously mentioned, claims 32, 34-35, 38-40, 42-44, 47-56, 58-66 and 68-83 have also been rejected under 35 U.S.C. § 102(a) as being anticipated by Ghori.

As discussed in the previously submitted responses, Ghori describes an upgrade central processing unit ("CPU") that includes handshake circuitry enabling such an upgrade CPU to communicate information about itself with the original CPU in the computer system. Upon system power-up or upon a reset, the original system CPU determines if there is a CPU in the upgrade socket and if so, what kind of CPU is present. The information about the upgrade CPU's identification and cooperative relationship capability is stored in either a discrete memory device incorporated into the interprocessor circuitry or burned directly into the read-only memory of the processor. See col. 4, lines 53-61. This information is used by the original system CPU to configure the system. Unless there is an upgrade CPU inserted in the upgrade socket, however, the computer system behaves normally, that is, without any modifications. Any change in the computer system's configuration is dependent on the presence of an upgrade CPU already added to the computer system.

Claim 32 is patentably distinct from the Ghori reference because it fails to disclose the combination of limitations recited by claim 32. For example, the Ghori reference fails to describe a method of selecting a compatible processor for addition to a multiprocessor computer that includes, among other things, executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the accessed processor compatibility information to determine the processors that are compatible with each current processor, and providing information identifying the processors that are compatible with each current processor before adding the new processor to the multiprocessor computer.

The Examiner argues that Ghori teaches that the BIOS provides such information before the processor is added to the multiprocessor computer as a functioning new processor, see the Office Action at page 25. This characterization of Ghori, however, is not correct. Ghori teaches determining if an upgrade CPU exists, providing information for that upgrade processor to the original system processor, and then configuring the computer system appropriately. Before the upgrade processor is added, the computer system operates under a first configuration and after the upgrade processor is added, the computer system operates under a second

configuration. Arguably, if an upgrade processor inserted in the upgrade socket is incompatible, the computer system will encounter an error during boot-up, thereby indicating an incompatible processor. However, this assumes that an upgrade processor is already inserted in the socket. No information identifying processors that are compatible with each current processor before adding the new processor to the multiprocessor computer is provided. At most, information indicating that an upgrade processor already added to the computer system is not compatible with the original system processor is provided.

Claim 40 is similarly patentably distinct from Ghori. Claim 40 recites a method of selecting a compatible processor for addition to a multiprocessor computer that includes, among other things, providing identifying information indicative of the identity of the new processor before adding the new processor to the multiprocessor computer, executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the accessed processor compatibility information to determine the processors that are compatible with each current processor, the computer program further comparing the identifying information for the new processor with the processors determined to be compatible with each current processor, and providing an indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer. Ghori relies on the presence of an upgrade CPU already added to the computer system to change its configuration. Otherwise, if no upgrade CPU is present, the configuration of the computer system is not changed. Everything about Ghori is keyed on whether an upgrade CPU is present or not.

Ghori fails to disclose the combination of limitations recited by claim 50. For example, Ghori fails to disclose a system for selecting a new processor for addition to a multiprocessor computer that includes, among other things, a fourth component that provides information identifying the processors that are compatible with each current processor before adding the new processor to the multiprocessor computer. Ghori at most describes a computer system that can detect incompatibility of an upgrade CPU that is already added to the computer system. No information identifying the processors that are compatible with each current process before adding a new processor to the computer system is provided, however.

Claim 60 is also patentably distinct from Ghori. Claim 60 recites a system for selecting a new processor for addition to a multiprocessor computer containing at least one current processor that includes, among other things, a second component allowing identifying information to be provided that identifies the new processor before adding the new processor to the multiprocessor computer, a fourth component coupled to first, second and third components

to compare the identifying information for the new processor with the compatibility information to determine processors that are compatible with each current processor, and a fifth component that provides an indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer. Ghori does not describe components for the computer system that allows identifying information to be provided that identifies the new processor before adding the new processor or that provides and indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer. Ghori describes altering configuration of the computer system based on whether an upgrade CPU processor is already present.

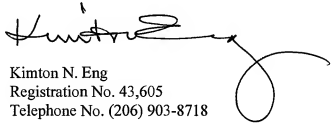
Claims 70 and 76 are also patentably distinct from Intel because it fails to described the combination of limitations recited by the respective claim. Claim 70 recites a computer-readable medium containing instructions for causing a computer system to use processor compatibility information to select a new processor for addition to a multiprocessor computer containing at least one current processor that includes, among other things, executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible with each current processor and providing information identifying the processors that are compatible with each current processor before adding the new processor to the multiprocessor computer. Claim 76 recites a computer-readable medium containing instructions for causing a computer system to use processor compatibility information to select a new processor for addition to a multiprocessor computer containing at least one current processor that includes providing identifying information indicative of the identity of the new processor before adding the new processor to the multiprocessor computer, executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible with each current processor, the computer program further comparing the identifying information for the new processor with the processors determined to be compatible with each current processor, and providing an indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer. The previous discussion of Ghori with respect to claims 32, 40, 50, and 60 are relevant to the patentability of claims 70 and 76 as well.

For the foregoing reasons, claims 32, 40, 50, 60, 70, and 76 are patentable over Ghori. The claims depending therefrom are similarly patentable based on their dependency from

a respective allowable base claim. Therefore, the Examiner's rejection of claims 32, 34, 35, 38-40, 42-44, 47-56, 58-66 and 68-83 under 35 U.S.C. 102(a) as being anticipated by Ghori should be withdrawn.

All of the claims pending in the present application in condition for allowance. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,
DORSEY & WHITNEY LLP



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